What is claimed is:

1. An LCD device, comprising:

a LCD panel;

a plurality of source drivers applying data signals to the LCD panel;

a plurality of gate drivers applying gate driving signals to the LCD panel;

a timing controller outputting at least two clock signals having different phases, the timing controller separately outputting data synchronized with each output signal; and

at least two data buses transmitting the data separately output from the timing controller to the source drivers.

2. The LCD device as claimed in claim 1, wherein a number of the data buses are in proportion to a number of clock signals output from the timing controller.

3. The LCD device as claimed in claim 1, wherein the timing controller outputs data synchronized with a rising edge time of each clock signal.

4. The LCD device as claimed in claim 1, wherein the timing controller outputs data synchronized with a falling edge time of each clock signal.

5. The LCD device as claimed in claim 1, wherein the timing controller outputs first and second clock signals having opposite phases to each other.

6. The LCD device as claimed in claim 1, wherein the timing controller outputs first, second and third clock signals, each having different phases to each another.

7. The LCD device as claimed in claim 4, wherein the source driver samples data in the falling edge time when the data synchronized with the rising edge time is output.

8. The LCD device as claimed in claim 5, wherein the source driver samples data in the rising edge time when the data synchronized in the falling edge timing is output.

9. The LCD device as claimed in claim 5, wherein odd numbered display data synchronized with the rising edge of the first clock signal is output, and even numbered display data synchronized with the rising edge of the second clock signal is output.

10. The LCD device as claimed in claim 6, wherein data for displaying R color synchronized with the rising edge of the first clock signal is output, data for displaying G color synchronized with the rising edge of the second clock signal is output, and data for displaying B color synchronized with the third clock signal is output.

11. A method for driving an LCD device having a timing controller transmitting digital data received from a system to each source driver comprising the steps of:

outputting at least two clock signals having different phases; and

separately outputting the digital data synchronized with respective clock signals per odd/even numbered data or R/G/B display data through different data buses.

12. The method as claimed in claim 11, wherein the data is synchronized with a rising edge of each clock signal.

13. The method as claimed in claim 12, wherein each source driver samples data synchronized with a falling edge if the data synchronized with a rising edge of each clock signal is output.

14. The method as claimed in claim 11, wherein the data synchronized with a falling edge of each clock signal is output.

15. The method as claimed in claim 14, wherein each source driver samples data synchronized with a rising edge if the data synchronized with a falling edge of each clock signal is output.

16. The method as claimed in claim 11, wherein two clock signals having different phases are used when the data is separately output according to odd and even numbered data, and three clock signals having different phases are used when the data is separately output according to R/G/B data.